OIPE JC43
MAY 1 1 1998
PATENT & TRADEMARK OFFICE

Amendments

Please amend the above-identified U.S. application as follows:

In the Claims:

Please amend claims 1, 2, 4, 6, 15, 19, 23, 24, 56 & 58 as set forth below.

1. (Amended) A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding and physically contacting the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface; and

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ

processed layer including via openings to at least some contact pads at the upper surfaces of said plurality of chips for electrical connection thereto.

16
~~2~~. (Amended) [The multichip module of claim 1,] A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ processed layer including via openings to at least some contact pads at the upper surfaces of said plurality of chips for electrical connection thereto; and

wherein said structural material has a thickness equal to a thickest chip of said plurality of chips such that the

45

upper surface of the structural material is substantially co-planar with the upper surface of the thickest chip to form said first substantially co-planar surface, and such that a lower surface of the structural material is substantially co-planar with a lower surface of said thickest chip of said plurality of chips to form a second substantially co-planar surface, said second substantially co-planar surface comprising said back surface.

17. (Amended) [The multichip module of claim 1,] A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ processed layer including via openings to at least some

46

contact pads at the upper surfaces of said plurality of chips for electrical connection thereto; and

wherein each chip of said plurality of chips has a common thickness, and wherein said structural material surrounding and mechanically interconnecting said chips in spaced planar relation comprises a thickness equal to said common thickness of said plurality of chips such that said second surface comprises a second substantially co-planar surface wherein the lower surface of said structural material is substantially co-planar with the lower surface of each chip of said plurality of chips, and wherein said first substantially co-planar surface comprising said front surface is parallel to said second substantially co-planar surface comprising said back surface.

4 ~~6~~. (Amended) The multichip module of claim 3 ~~5~~, wherein said multi-layer structure further comprises a release layer disposed over said in situ processed layer, said release layer being [thermally or chemically] removable without removing said in situ processed layer, said release layer comprising one of a thermoplastic material or a solventable material.

18 ~~15~~. (Amended) [The multichip module of claim 14,] A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, a lower surface, and at least one contact pad at said upper surface;

a structural material surrounding the at least one side surface of each chip of said plurality of chips and mechanically interconnecting in spaced, planar relation said plurality of chips, said structural material having an upper

47

surface substantially co-planar with an upper surface of each chip of said plurality of chips to form a first substantially co-planar surface, said first substantially co-planar surface comprising a front surface, and such that a lower surface of said structural material is substantially parallel with a lower surface of each chip of said plurality of chips to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material mechanically interconnecting said plurality of chips, said in situ processed layer including via openings to at least some contact pads at the upper surfaces of said plurality of chips for electrical connection thereto;

wherein each chip of said plurality of chips comprises a bare integrated circuit chip; and

wherein each chip of said plurality of chips has an equal thickness such that the upper surface of each chip is co-planar with said front surface and the lower surface of each chip is co-planar with said back surface, said back surface comprising a planar main surface of the multichip module.

---

20. (Amended) An integrated circuit chip module comprising:

an integrated circuit chip comprising a bare chip having a substrate, active circuitry associated with said substrate, an upper surface and a lower surface, said integrated circuit chip further comprising multiple electrical contact pads at said upper surface electrically coupled to said active circuitry, said integrated circuit

chip further having at least one side with a width defined by said upper surface and said lower surface;

a structural material surrounding and physically contacting said at least one side of said integrated circuit chip, said structural material having a top surface substantially co-planar with said upper surface of said integrated circuit chip to form a first surface, said first surface comprising a front surface, and said structural material having a bottom surface substantially parallel with said lower surface of said integrated circuit chip to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material surrounding said at least one side of said integrated circuit chip, said in situ processed layer including at least one via opening to at least one contact pad of said multiple electrical contact pads at the upper surface of said integrated circuit chip; and

a metallization structure comprising metallization disposed within said at least one via opening electrically connecting to said at least one contact pad of said integrated circuit chip.

25

~~23~~. (Amended) [The integrated circuit chip module of claim 20,] An integrated circuit chip module comprising:

an integrated circuit chip comprising a bare chip having a substrate, active circuitry associated with said substrate, an upper surface and a lower surface, said integrated circuit chip further comprising multiple

49

electrical contact pads at said upper surface electrically coupled to said active circuitry, said integrated circuit chip further having at least one side with a width defined by said upper surface and said lower surface;

a structural material surrounding said at least one side of said integrated circuit chip, said structural material having a top surface substantially co-planar with said upper surface of said integrated circuit chip to form a first surface, said first surface comprising a front surface, and said structural material having a bottom surface substantially parallel with said lower surface of said integrated circuit chip to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material surrounding said at least one side of said integrated circuit chip, said in situ processed layer including at least one via opening to at least one contact pad of said multiple electrical contact pads at the upper surface of said integrated circuit chip;

a metallization structure comprising metallization disposed within said at least one via opening electrically connecting to said at least one contact pad of said integrated circuit chip;

wherein said in situ processed layer comprises a photo-patternable dielectric material; and

wherein said bottom surface is substantially co-planar with said lower surface of said integrated circuit chip.

50

24. (Amended) [The integrated circuit chip module of claim 20,] An integrated circuit chip module comprising:

an integrated circuit chip comprising a bare chip having a substrate, active circuitry associated with said substrate, an upper surface and a lower surface, said integrated circuit chip further comprising multiple electrical contact pads at said upper surface electrically coupled to said active circuitry, said integrated circuit chip further having at least one side with a width defined by said upper surface and said lower surface;

a structural material surrounding said at least one side of said integrated circuit chip, said structural material having a top surface substantially co-planar with said upper surface of said integrated circuit chip to form a first surface, said first surface comprising a front surface, and said structural material having a bottom surface substantially parallel with said lower surface of said integrated circuit chip to form a second surface, said second surface comprising a back surface;

an in situ processed layer disposed on said front surface, said in situ processed layer comprising a material different from said structural material surrounding said at least one side of said integrated circuit chip, said in situ processed layer including at least one via opening to at least one contact pad of said multiple electrical contact pads at the upper surface of said integrated circuit chip;

a metallization structure comprising metallization disposed within said at least one via opening electrically connecting to said at least one contact pad of said integrated circuit chip;

wherein said in situ processed layer comprises a photo-patternable dielectric material; and

wherein said back surface comprises an exposed planar main surface of said integrated circuit chip module.

27

~~56~~. (Amended) A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, and a lower surface; and

structural material surrounding and physically contacting the at least one side surface of each chip of said plurality of chips to mechanically interconnect in spaced planar relation said plurality of chips, said structural material having an upper surface co-planar with the upper surfaces of said plurality of chips, wherein a co-planar front surface is defined thereby, and wherein a lower surface of said structural material is substantially parallel with the lower surfaces of the plurality of chips, thereby defining a back surface.

28

~~57~~. (Amended) [The multichip module of claim 56,] A multichip module comprising:

a plurality of chips, each chip comprising an unpackaged chip having at least one side surface, an upper surface, and a lower surface;

structural material surrounding the at least one side surface of each chip of said plurality of chips to mechanically interconnect in spaced planar relation said plurality of chips, said structural material having an upper surface co-planar with the upper surfaces of said plurality

52

of chips, wherein a co-planar front surface is defined thereby, and wherein a lower surface of said structural material is substantially parallel with the lower surfaces of the plurality of chips, thereby defining a back surface; and

wherein the lower surface of the structural material is substantially co-planar with the lower surfaces of the plurality of chips.

Kindly add new claims 60 & 61 as follows:

--60. The multichip module of claim 1, wherein said structural material surrounds and physically contacts the at least one side surface of each chip so that there is no space between said structural material and said at least one side surface of each chip of said plurality of chips.--

--61. The integrated circuit chip module of claim 19, wherein said structural material surrounds and physically contacts the at least one side surface of said integrated circuit chip so that there is no space between said structural material and said at least one side surface of said integrated circuit chip.--

Remarks

Entry of this amendment, reconsideration of the application, and allowance of all claims pending herein are respectfully requested. By this amendment, claims 1, 6, 19 and 56 are amended and new claims 60 & 61 are added to more particularly point out and distinctly claim the subject matter of the present invention. Objected to claims 2, 4, 6, 15, 23, 24 & 58 are rewritten in independent form pursuant to the Examiner's suggestion in the first Office Action. Claims 1-24 & 56-61 are now pending. Of